REMARKS

Applicants respectfully request entry of the Amendments to the Claims set forth above. The changes are fully supported in the specification, and thus there is no issue of new matter. New Claims 40-47 are supported by original Claims 18 and 30 and by the specification at paragraph [0060].

Applicants reserve the right to file divisional and/or continuation applications containing claims directed to all or part of the subject matter described in the instant application, as well as the subject matter of any claims amended or canceled at any time during the prosecution of this application, and thus unclaimed subject matter is not dedicated to the public.

Information Disclosure Statement

Applicants acknowledge receipt of the initialed PTO-1449 form listing the 83 references submitted to the Office on April 24, 2002. However, Applicants have not yet received the initialed PTO-1449 form listing the three references submitted to the Office on August 27, 2002, nor the initialed PTO-1449 form listing the three references submitted to the Office on November 25, 2002. Applicants respectfully request copies of the initialed PTO-1449 forms from these latter submissions.

Claim Rejections - 35 U.S.C. §103(a)

Claims 1-39 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Yu et al. (U.S. Patent No. 6,281,559), further in view of Nakabayashi et al. (U.S. Patent No. 6,319,782), Shiota et al. (U.S. Patent No. 5,879,970) and Madhukar (U.S. Patent No. 6,444,512). Applicants respectfully traverse these rejections.

Yu does not disclose forming a high-k material over a semiconductor substrate as claimed. The Office states that Yu discloses depositing a silicon-containing seed layer (524, fig. 20) over a high-k material under seed phase conditions. However, Yu discloses that the dielectric layer 526 (onto which Yu deposits the seed layer 524) is silicon dioxide, silicon oxide nitride (SiON), or an unspecified nitride material. *See* column 11, lines 12-14. Neither silicon dioxide nor SiON is a high-k material as claimed. High-k materials have a k value greater than about 7 and thus have a higher dielectric constant than either silicon dioxide or silicon nitride, as discussed in the specification at, e.g., paragraphs [0015], [0019], and [0060]. High-k materials

also have a k value greater than that of SiON. In this respect, Applicants respectfully direct the attention of the Office to U.S. Patent No. 5,587,344 ("Ishikawa"), a copy of which is provided herewith for the convenience of the Office. As indicated in Ishikawa at column 6, lines 32-44 and figure 6, conventional silicon dioxide has a dielectric constant of about 4.1 and SiON has a dielectric constant in the range of 3.6 to 4.4. Therefore, Yu does not disclose, teach or suggest a high-k material as claimed.

The Office states that Madhukar discloses a high-k layer and that one of ordinary skill in the art would be motivated to combine Madhukar with Yu (along with Nakabayahi and Shiota) because the high-k layer allows for the use of a thicker gate dielectric film without adversely affecting the electrical and capacitive characteristics of the film.

Applicants respectfully disagree because Madhukar teaches away from depositing a polysilicon layer on a high-k material. The Office notes that Madhukar's gate dielectric 108 may be a high k material. However, Madhukar deposits a first metal 110 and a second metal 114 over the gate dielectric 108, see column 2, lines 54-55; column 3, lines 25-28; and figures 1 and 3, not a silicon-containing seed layer as claimed. Madhukar states that depositing first and second metals 110, 114 over the gate dielectric 108 avoids the difficulties associated with polysilicon gates:

> It will be appreciated by those in the field having the benefit of this disclosure that the use of a first metal 110 of a first metal type in contact with gate dielectric 108 for transistors of a first conductivity type coupled with the use of a second metal 114 of a second metal type (where the first and second metal types differ) in contact with gate dielectric layer 108 for the second type of transistors enables the threshold voltage alignment of n-channel and p-channel devices while avoiding difficulties associated with polysilicon gates including boron diffusion, polysilicon depletion effects, and potential incompatibility with alternative gate dielectric films.

See Madhukar at column 4, lines 11-21 (emphasis added). Since Yu seeks to deposit a polysilicon layer 524 over the dielectric layer 526, Madhukar would deter, not motivate, one skilled in the art from employing a high-k material as the dielectric layer 526 because of the "difficulties associated with polysilicon gates."

Applicants respectfully submit that the Office's proposed combination of Yu and Madhukar is improper: "It is improper to combine references where the references teach away from their combination." M.P.E.P. § 2145 (X)(D)(2) (citing *In re Grasselli*, 713 F.3d 731, 743,

218 U.S.P.Q. 769, 779 (Fed. Cir. 1983)). Yu discloses depositing a polysilicon seed layer 524 over a silicon dioxide or SiON dielectric layer 526. Ishikawa establishes that silicon dioxide and SiON are not high-k materials, and thus that dielectric layer 526 is not a high-k material. The Office looks to Madhukar for the disclosure of a high-k material, but Madhukar teaches away from replacing Yu's dielectric layer 526 with a high-k material because of the difficulties that would be encountered as a result of Yu's subsequent deposition of polysilicon layer 524. Therefore, there is no motivation to combine Yu and Madhukar as proposed by the Office.

The Office cites Nakabayashi as disclosing a higher order silane gas, a seed phase deposition rate that is less than 500 Å/min., and a bulk phase deposition rate that is greater than 500 Å/min., and cites Shiota as disclosing a non-hydrogen carrier gas. However, Applicants respectfully submit that neither Nakabayashi nor Shiota, each alone or in combination, cure the above-noted deficiencies of Yu.

Applicants respectfully submit that the Office has not established a *prima facie* case of obviousness because there is no motivation to modify Yu to meet the instant claims. *See* M.P.E.P. § 2143. Rather than establishing a motivation to combine, Madhukar provides evidence of nonobviousness because it states the conventional wisdom regarding the difficulties associated with polysilicon gates over high-k materials. Such difficulties are well known to those skilled in the art, as discussed in the Background section of the instant specification at, e.g. paragraphs [0007], [0008] and [0017]. Thus, Applicants have proceeded against the conventional wisdom by depositing a silicon-containing layer over a high-k material. "Proceeding contrary to accepted wisdom is evidence of non-obviousness." M.P.E.P. § 2145 (X)(D)(3).

Therefore, because a *prima facie* case of obviousness has not been established, Applicants respectfully request reconsideration and withdrawal of the rejection of Claims 1-39 under 35 U.S.C. §103(a) as being unpatentable over Yu, further in view of Nakabayashi, Shiota, and Madhukar.

Conclusion

Applicants respectfully submit that the instant claims satisfy the requirements for patentability in view of all of the prior art cited, searched, and considered by the Office, including the three references submitted to the Office on August 27, 2002, and the three references

submitted to the Office on November 25, 2002, and respectfully submit that the instant application is in condition for allowance, early notification of which would be appreciated. Should the Office disagree, Applicants respectfully request a telephonic interview to discuss any outstanding issues. The Office is respectfully invited to contact Applicants' representative at the telephone number provided below in this regard.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 4/8/03

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AMEND

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